CLAIMS

What is claimed is:

1. An error correction coding apparatus comprising:

a parity check matrix generation unit which generates a parity check matrix having a number of elements having a value of 1 in each row thereof, having a predetermined number of elements having a value of 1 in each column thereof, and having the other elements having a value of 0;

a parity check matrix adjustment unit which receives the parity check matrix from the parity check matrix generation unit, searches the parity check matrix for a cycle forming group of four elements positioned at respective vertexes of a rectangle and having a value of 1, and when there is at least one cycle forming group, replaces the value of 1 of at least one element of the cycle forming group with the value 0 of another element, to output an adjusted parity check matrix without a cycle forming group therein; and

an LDPC coding unit which receives the adjusted parity check matrix from the parity check matrix adjustment unit and receives an m-bit message word to perform LDPC coding.

2. The error correction coding apparatus of claim 1, wherein the parity check matrix adjustment unit comprises:

a matrix element check unit which receives the parity check matrix from the parity check matrix generation unit, searches the parity check matrix for a plurality of cycle forming groups and outputs information on positions (w1, x1), (w1, y1), (z1, x1) and (z1, y1) of the respective elements of a first cycle forming group and information on positions (w2, x2), (w2, y2), (z2, x2) and (z2, y2) of the respective elements of a second cycle forming group; and

a matrix element shifting unit which receives the information on positions of the respective elements of the first cycle forming group and the information on positions of the respective elements of the second cycle forming group from the matrix element checking unit, shifts one element S_{ij} having a value of 1 of the first cycle forming group, where i=w1 or z1 and j=x1 or y1, to one of (i, x2) and (i, y2) and shifts one element Q_{kl} having a value of 1 of the second cycle forming group existing on a column to which S_{ij} is shifted, to (k, j), thereby removing the first and second cycle forming groups from the parity check matrix, and wherein, when two other cycle forming groups are present in the parity check matrix, the parity check matrix adjustment unit operates removes them so as to generate the adjusted parity check matrix.

3. The error correction coding apparatus of claim 1, wherein the parity check matrix adjustment unit comprises:

a matrix element check unit which receives the parity check matrix from the parity check matrix generation unit, searches for a plurality of cycle forming groups existing in the parity check matrix, and outputs information on positions (w1, x1), (w1, y1), (z1, x1) and (z1, y1) of elements constituting a first cycle forming group and information on positions (w2, x2), (w2, y2), (z2, x2) and (z2, y2) of elements constituting the second cycle forming group; and

a matrix element shifting unit which receives the information on positions of the respective elements of the first cycle forming group and the information on positions of the respective elements of the second cycle forming group from the matrix element checking unit and shifts one element S_{ij} having a value of 1 of the first cycle forming group, wherein i=w1 or z1 and j=x1 or y1, to one of (w2, j) and (z2, j) and shifts one element Q_{kl} having a value of 1 of the second cycle forming group existing on a row to which S_{ij} is shifted, where k=w2 or z2 and l=x2 or y2, to (i, l), thereby removing the first and second cycle forming groups from the parity check matrix, and wherein, when two other cycle forming groups are present in the parity check matrix, the parity check matrix adjustment unit removes them so as to generate the adjusted parity check matrix.

4. The error correction coding apparatus of claim 1, wherein the LDPC coding unit determines parity information x_i (i=1, 2,...p) as elements of the matrix X satisfying the following equation:

$H \times M = 0$

wherein X is a (m+p) ×1 matrix $\begin{pmatrix} k_1 \\ k_2 \\ . \\ . \\ . \\ k_m \\ x_1 \\ x_2 \\ . \\ . \\ . \\ x_p \end{pmatrix}$

and outputs a codeword having the parity information x_i added to the message word k_i (i=1, 2,...m).

5. The error correction coding apparatus of claim 2, wherein the matrix element shifting unit receives the parity check matrix from the parity check matrix generation unit and shifts an element S_{ij} having a value of 1 of the first cycle forming group, wherein i=w1 or z1 and j=x1 or y1, the element S_{ij} has a value of 1 and is shifted to another position when the value of 1 exists at the shifted position.

6. The error correction coding apparatus of claim 2, wherein the matrix element shifting unit receives the parity check matrix from the parity check matrix generation unit and shifts another element having a value of 1 of the first cycle forming group, wherein i=w1 or z1 and j=x1 or y1, the element has a value of 1 and is shifted to another position when the value of 1 exists at the shifted position.

7. The error correction coding apparatus of claim 2, wherein the matrix element shifting unit receives the parity check matrix from the parity check matrix generation unit and shifts an element S_{ij} having a value of 1 of the first cycle forming group, wherein i=w1 or z1 and j=x1 or y1, the element S_{ij} has a value of 1 and is shifted to another position when a third cycle forming group is newly generated by the shift of the element S_{ij}.

8. The error correction coding apparatus of claim 2, wherein the matrix element shifting unit receives the parity check matrix from the parity check matrix generation unit and shifts another element having a value of 1 of the first cycle forming group, wherein i=w1 or z1 and j=x1 or y1, the element having a value of 1 and is shifted to another position when a third cycle forming group is newly generated by the shift of the another element.

9. The error correction coding apparatus of claim 2, wherein the matrix element shifting unit receives the parity check matrix from the parity check matrix generation unit, shifts an element S_{ij} having element value 1 of the first cycle forming group, where i=w1 or z1 and j=x1 or y1, to another position, and when the first cycle forming group and the second cycle forming group are not removed, requests from the matrix element check unit position information for another pair of cycle forming groups to remove.

10. The error correction coding apparatus of claim 2, wherein, when all cycle forming groups existing in the parity check matrix are not removed, the parity check matrix shifting unit requests from the parity check matrix generation unit a new parity check matrix.

11. An error correction coding method comprising:

generating a parity check matrix having a number of elements having a value of 1 in each row thereof, having a number of elements having a value of 1 in each column thereof, and having the other elements having a value of 0;

receiving the parity check matrix, searching the parity check matrix for a cycle forming group of four elements positioned at the respective vertexes of a rectangle and having a value of 1, and when there is at least one cycle forming group, replacing the value of 1 of at least one element of the cycle forming group with the value 0 of another element, to output a adjusted parity check matrix without a cycle forming group therein; and

receiving the modified parity check matrix and receiving an m-bit message word to perform LDPC coding.

12. The error correction coding method of claim 11, wherein the receiving the parity check matrix comprises:

receiving the parity check matrix, searching the parity check matrix for the plurality of cycle forming groups and outputting information on positions (w1, x1), (w1, y1), (z1, x1) and (z1, y1) of the respective elements of a first cycle forming group and information on positions (w2, x2), (w2, y2), (z2, x2) and (z2, y2) of the respective elements of a second cycle forming group;

shifting one element S_{ij} having a value of 1 of the first cycle forming group, wherein i=w1 or z1 and j=x1 or y1, to one of (i, x2) and (i, y2) and shifting one element Q_{kl} having a value of 1 of the second cycle forming group existing on a column to which S_{ij} is shifted, to (k, j), thereby removing the first and second cycle forming groups; and

repeating the cycle forming group removing with respect to two another cycle forming groups to generate the modified parity check matrix.

13. The error correction coding method of claim 11, wherein the receiving the parity check matrix comprises:

receiving the parity check matrix, searching the parity check matrix for a plurality of cycle forming groups, and outputting information on positions (w1, x1), (w1, y1), (z1, x1) and (z1, y1) of elements constituting a first cycle forming group and information on positions (w2, x2), (w2, y2), (z2, x2) and (z2, y2) of elements constituting a second cycle forming group, thereby checking matrix elements;

shifting one element S_{ij} having a value of 1 of the first cycle forming group, wherein i=w1 or z1 and j=x1 or y1, to one of (w2, j) and (z2, j), and shifting one element Q_{kl} having a value of 1 of the second cycle forming group existing on a column to which S_{ij} is shifted, wherein k=w2 or z2 and l=x2 or y2, to (i, l), thereby removing the first and second cycle forming groups;

repeating the shifting one element with respect to two another cycle forming groups to generate the modified parity check matrix.

14. The error correction coding method of claim 11, wherein the receiving the modified parity check matrix comprises determining the parity information x_i, where i=1,2...p, as elements of the matrix X satisfying the following equation:

$H \times M = 0$

wherein X is a (m+p) ×1 matrix $\begin{pmatrix} k_1 \\ k_2 \\ . \\ . \\ . \\ k_m \\ x_1 \\ x_2 \\ . \\ . \\ . \\ x_p \end{pmatrix}$

and outputting a codeword having the parity information x_i added to the message word k_i (i=1, 2,...m).

15. The error correction coding method of claim 12, wherein the shifting one element comprises receiving the parity check matrix, and when the value of 1 exists at the shifted position when the element S_{ij} has a value of 1 of the first cycle forming group, wherein i=w1 or z1 and j=x1 or y1, and shifting the element S_{ij} having a value of 1 to another position.

16. The error correction coding method of claim 12, wherein the shifting one element comprises receiving the parity check matrix C, and if the element value 1 exists at the shifted position in the case of shifting an element S_{ij} having element value 1 of the first cycle forming group, where i=w1 or z1 and j=x1 or y1, and shifting another element having element value 1 to another position.

17. The error correction coding method of claim 12, wherein the shifting one element comprises receiving the parity check matrix C, and if a third cycle forming group is generated in the case of shifting an element S_{ij} having element value 1 of the first cycle forming group, where i=w1 or z1 and j=x1 or y1, and shifting the element S_{ij} having element value 1 to another position.

18. The error correction coding method of claim 12, wherein the shifting one element comprises receiving the parity check matrix C, and wherein, when a third cycle forming group is generated in the case of shifting an element S_{ij} having element value 1 of the first cycle forming group, where i=w1 or z1 and j=x1 or y1, shifting another element having element value 1 to another position.

19. The error correction coding method of claim 12, wherein the shifting one element comprises receiving the parity check matrix C, shifting an element S_{ij} having element value 1 of the first cycle forming group, where i=w1 or z1 and j=x1 or y1, to another position and, when the first cycle forming group and the second cycle forming group are not removed, receiving another pair of cycle forming groups to perform removing the pair of cycle forming groups.

20. The error correction coding method of claim 12, further comprising generating a new parity check matrix when all cycle forming groups existing in the parity check matrix are not removed and repeating the receiving the parity check matrix, shifting one element S_{ij}, and repeating the cycle forming group removing.

21. A computer readable medium encoded with processing instructions for performing an error correction coding method comprising:

generating a parity check matrix having a number of elements having a value of 1 in each row thereof, having a number of elements having a value of 1 in each column thereof, and having the other elements having a value of 0;

receiving the parity check matrix, searching the parity check matrix for a cycle forming group of four elements, the four elements positioned at the respective vertexes of a rectangle and having a value of 1, and when there is at least one cycle forming group, replacing the value of 1 of at least one element of the cycle forming group with the value 0 of another element, to output a adjusted parity check matrix without a cycle forming group therein; and

receiving the modified parity check matrix and receiving a m-bit message word to perform LDPC coding.

22. An error correction coding apparatus comprising:

a parity check matrix generator which generates a parity check matrix, having one or more rows and one or more columns, a number of elements of a first value in each row and each column and a number of elements of a second value;

a parity check modifier which searches the parity check matrix for a cycle forming group of four elements positioned at each of the verticies of a rectangle and being of the first value and, when at least one cycle forming group is found, replaces the value of at least one element of each of the one ore more cycle forming groups with the second value, to output a modified parity check matrix without a cycle forming group therein; and

a low density parity code (LDPC) coder which receives an m-bit message word to perform LDPC coding and performs LDPC coding using the adjusted parity check matrix.

23. A computer readable storage medium encoded with processing instructions for performing an error correction coding method comprising:

generating a parity check matrix, having one or more rows and one or more columns, a number of elements of a first value in each row and each column and a number of elements of a second value;

searching the parity check matrix for a cycle forming group of four elements positioned at each of the vertices of a rectangle and being of the first value and, when at least one cycle forming group is found, replaces the value of at least one element of each of the one or more cycle forming groups with the second value, to output a modified parity check matrix without a cycle forming group therein; and

receiving an m-bit message word to perform low density parity code (LDPC) coding and performing LDPC coding using the adjusted parity check matrix.